International Journal of Technology and Engineering System (IJTES)
Vol 6. No.3 – Jan-March 2014 Pp. 208-214
©gopalax Journals, Singapore
available at : www.ijcns.com
ISSN: 0976-1345

IMPLEMENTATION OF FSM BASED MEMORY ARCHITECTURE FOR REDUCING MEMORY FAULT IN OFDM SYSTEM

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ABSTRACT

The growing density of integration and the increasing percentage of system-on-chip area occupied by embedding memories have led to an increase in the expected number of memory faults. The FSM based soft memory repair strategy proposed in this paper employs to an provides higher operating frequency and better FPGA resource utilization. Use of FPGA's embedded memory offers advantages like reduced access time, lesser occupancy of circuit board and lower power consumption. The main objective of this project is to develop a cost-effective memory repair solution for a SoC-based OFDM receiver containing embedded memory. Linear-Density Parity-Check (LDPC) decoder was implemented to demonstrate the architecture. This decoder can achieve a throughput. A successful repair technique to introduce minimal area, speed, and power overhead and provide acceptable error tolerance as measured by the Bit Error Rate (BER) and the Packet Error Rate (PER) at the Quasi-Error-Free (QEF), and also introduces a single multiplexer delay overhead and a configurable area overhead of M/i bits, where M is the number of memory rows and i is an integer from 1 to M, inclusive. The repair strategy achieves a measured 0.52 dB gain improvement in the presence of stuck-at memory faults for an additive white Gaussian noise channel.

Index Terms— Interleaver, orthogonal frequency-division multiplexing receiver, Finite state machine, soft memory repair, system-on-chip.

I. INTRODUCTION

The International Technology road map for semi-conductor project (ITRS) that embedded memories will occupy an increasing percentage of a system-on-chip (SoC) area [1]. As a result, the overall SoC yield is becomes increasingly depend- ent on memory yield. The high density of integration enabled by diminishing transistor geometrics makes embedded memories particularly susceptible to manufacturing faults. Manufacturing process variations also dramatically reduce the reliability and yield of fabricated SoCs. In this paper, in order to achieve a better error performance. Hence, demand will increase for embedded memories that consume relatively large die areas but are highly adaptable to internal failures. Such designs can help control costs of design Verification and design of testing.

FSM soft repair strategies that utilize a redundant resource such as spare rows and columns to repair faulty memory cells [7]–[9] introduce area overhead and contribute to the cost of the SoC. Even though techniques such as divided word and bit lines [10] and redundancy analysis schemes [11] attempt to reduce the overhead, not all memory cells contribute equally to system-level performance. For example, in baseband signal processing [1]-[3], a faulty least significant bit (LSB) when compared to a most significant bit (MSB) fault leads to smaller performance degradation as measured by system parameters[7] such as the bit error rate (BER).

Similarly, memories that store data prior to filtering and error correction operations exhibit [12] higher fault tolerance due to a higher degree of randomness as measured by entropy. This variation in sensitivity to memory faults can be exploited to minimize the impact of faults, whereby faulty memory blocks with high sensitivity to faults [15] are permuted with functional blocks of low fault sensitivity without [4] resorting to redundant rows and columns. Furthermore, LDPC decoder used to achieve throughput. at the system level can be used to save the area overhead[11].

The Finite state machine based address generator operates at higher frequency and can provide better FPGA resource utilization [9]. Use of internal memory always provides better results in terms of memory access time, power consumption and real estate occupancy of circuit board[13] compared to external memory is a model of computation based on a hypothetical machine made of one or more states. Only a single state can be active at the same time, so the machine must transition from one state to another in order to perform different actions A finite-state machine is a model used to represent and control execution flow.

The proposed FSM soft memory repair strategy eliminates redundant rows and columns in favor of FEC and improves decoding performance in the presence of memory faults by permuting the data so as to minimize the impact of memory faults on system performance as measured by the BER and those memory architecture was implemented on OFDM architecture measured of an area and power utilization.

To improves decoding performance in the presence of memory faults by permuting the data so as to minimize the impact of memory faults on system performance as measured by the BER and also implemented on OFDM architecture measured of an area and power utilization. In view of the in order to achieve a better error performance, can further reduce the complexity and memory requirements.

In many statistical signal processing applications, such as digital communications and video processing, a certain number of errors can be tolerated without a noticeable degradation in performance or user experience of the device [12]. Algorithms considerable area savings can be achieved.

II. SYSTEM OVERVIEW

Orthogonal frequency-division multiplexing (OFDM) multicarrier transmission schemes find wide application in wire- line as well as wireless standards. The design differences across OFDM receivers supporting different standards can be abstracted and grouped into stream, block, and FEC modules. The stream modules perform synchronization and mode estimation functions. The block modules compute the fast Fourier transform (FFT) and carry out channel estimation and equalization.

The FEC modules perform de-interleaving and FEC operat- ions, as illustrated by the soft-output LDPC decoders. The area occupied by embedded memory in future OFDM receivers is expected to rise, as well as the fault density. Thus, to address the problem of the increasing number of manufacturing faults, a generic model of an embedded- memory OFDM receiver.

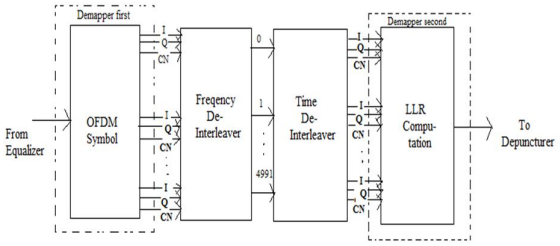

Fig. 1. FTDI Block Diagram.

Without loss of generality, the proposed memory repair strategy is illustrated on an ISDB-T OFDM receiver, and more specifically in the frequency-time de-interleaver (FTDI) because of its large memory requirements as described in the ISDB-T standard [13] and highlighted in Fig. 1. The SRAM- based FTDI occupies more than half of the SoC core area.

Thus, it is the single largest area contributor. In addition, due to the high density of embedded SRAM, the probability of SRAM errors per unit area caused by manufacturing faults is several times higher than standard cell digital logic. A static memory retains information as long as power is applied, while a dynamic memory can lose information even when power is continuously applied. Static RAMs (SRAMs) are flip-flops that, with their two stable states, can remain in a given state indefinitely, without need for refresh, as long as power is applied; that is, they are static but volatile.

A. Frequency Time De-Interleaver

A block diagram of the frequency and time convolution de-interleaver is shown in Fig. 2. An Top view of an interleaver changes the order of symbols before trans-mission to convert long burst errors into shorter bursts or random errors that can be more easily corrected by the error correction logic [14], [15]. Interleavers are characterized by an encoding delay and storage.

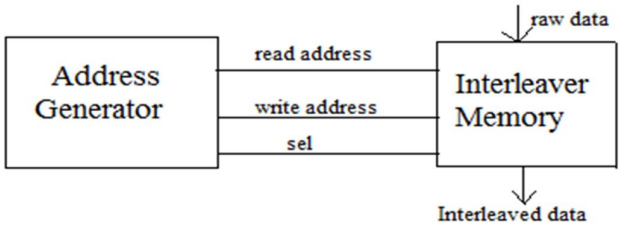

Fig. 2. Top view of Interleaver.

A block interleaver of degree m formats the input symbol vector of length m × n into a rectangular array of m rows and n columns such that a consecutive pair of symbols at the input appears m symbols apart at the output. The rectangular array is filled row by row and the interleaver output is read out column by column.

III. MEMORY FAULT STRATEGY

In order to develop an efficient fault-tolerant strategy for embedded-memory baseband signal processing systems, it is important to understand the

nature of memory faults and to quantify their effect on yield.

A. Fault Model

An embedded memory consists of three main functional blocks: the memory array, the address decoder, and the read and write circuits.

- *Stuck at Faults (SAFs)*: A memory cell value is stuck- at-zero (s-a-0) or stuck-at-one (s-a-1) and the contents of the cell cannot be altered.
- *Stuck Open Faults (SOFs)*: A memory cell is stuck open and the contents of the cell cannot be accessed.
- *Data Retention Faults (DRFs)*: A memory cell fails to retain its value after a certain period of time.
- *Transition Faults (TFs)*: A memory cell fails in at least one $0 \rightarrow 1$ or $1 \rightarrow 0$ transitions.
- *Coupling Faults (CFs)*: A state, an operation, or a transition because of a write to one memory cell (coupling cell) affecting the value of another memory cell (coupled cell).

B. Fault Repair Strategy

The proposed repair strategy saves implementation costs by eliminating redundant rows and columns or local error correction, and improving decoding performance in the pres- ence of memory faults by permuting the data so as to minimize the impact of memory faults on system performance as measured by the BER.

A sensitivity coefficient ζ is assigned for each bit in a memory word as a difference in BER caused by a SAF compared to the fault-free memory cell, normalized to 1 where the Eq. 1 subscripts *SA* and *FF* represent stuck-at and fault-free respectively, and *C* is normalization constant.

$$\zeta = \frac{1}{C} (BER_{SA} - BER_{FF}) \qquad (1)$$

The BER is the number of received bits of a data stream over sa communication channel that has been altered due to the noise, interference, distortion errors. PER is the number of incorrectly received data packets divided by the total number of received packets.

C. FSM Representation

Combinational logic units are a type of logic circuit whose output is a pure function of the present input only. Finite State Machines, used in sequential logic, have outputs that depend on both the present input as well as the history of the input. A sequential logic unit which,

- Takes an input and a current state
- Produces an output and a new state

It is called a Finite State Machine because it can have, at most, a finite number of states. It is composed of a combinational logic unit and flip-flops placed in such a way as to maintain state information.

Table.1. FSM state transition table.

Input Current State	$Input_0$	$Input_1$	….	$Input_n$
$State_0$	Next State / Output	….		Next State / Output
$State_1$	….	….		….
….	….	….		….
$State_n$	….	….		….

It can be represented using a **state transition table** which shows the current state, input, any outputs, and the next state. It can also be represented using a **state diagram** which has the same information as the state transition diagram.

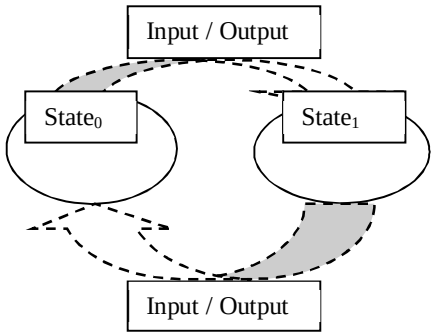

Fig. 3. FSM State Diagram.

IV. MEMORY ARCHITECTURE

An architecture of the proposed FSM soft memory repair technique. The proposed technique interfaces with MBIST via data and test address bus lines as well as an error signal (cur_err_out) indicating a mismatch during an MBIST march test.

The FTDI memory is organized internally into 1K rows. Therefore, the maximum size of the row address fault register is 1024. However, to reduce area overhead, a single bit in the row address fault register can be used to track multiple rows. Thus, the size of the row address fault register can be reduced by i, where i, is an integer between 1 and M, equal to the number of memory rows assigned to a single bit of the row address fault register.

In this decoder, a bidirectional forward-backward recursion is adopted to improve the decoding latency, and layered scheduling is used to reduce the number of iterations for a given performance. Consequently, the throughput can be increased.

The proposed technique introduces a single multiplexer delay overhead since the only additional data.

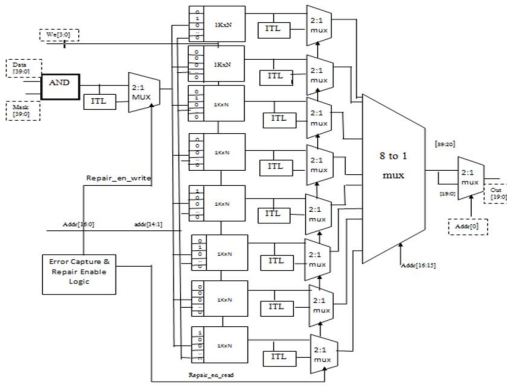

Fig. 4. Proposed Memory Repair architecture.

In the MBIST mode, the error capture and repair enable logic is used to: 1) capture externally the serial output of the error register; 2) examine its contents for the location of faults in both high- and low-sensitivity regions; and 3) set the corresponding bit of the row address fault register if the higher sensitivity region has at least one fault while the lower sensitivity region is fault free.

In the functional mode, the row address fault register is accessed on every read and write operation and, if the current row address is labeled faulty, the regions of high and low sensitivity are permuted by the repair interleave (ITL) logic and output through the 2-to-1 MUX controlled by repair enable signals path delay is due to the 2-to-1 MUX during write and read operations, while the ITL logic performs a negligible delay permutation operation. The proposed technique introduces a configurable area overhead of *M*/ i bits, where M is the number of memory rows and i is an integer from 1 to M , inclusive. When i = 8 and M = 1024, due to the external-to memory row address fault register consisting of M/ i =1024/8 =128 flip flops was used.

V. SYSTEM INTEGRATION

Orthogonal frequency division multiplexing (OFDM) technique is currently an active field of research in the area of communication and has been used to develop wireless local area network (WLAN) systems To make the system work efficiently, reestablishment of the orthogonally condition at the receiver is necessary. This is done by the so called Inner Receiver (IRx) Block shown In essence, two main operations are carried out inside the IRx, namely signal acquisition and channel correction.

In this LDPC decoder, a bidirectional forward-backward recursion is adopted to improve the decoding latency, and layered scheduling is used to reduce the number of iterations for a given performance. Consequently, the throughput can be increased. In addition, we propose a compression technique to reduce the memory requirements and, hence, the area to be implemented in this architecture.

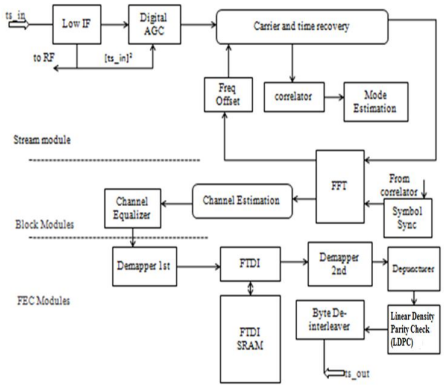

Fig .5. OFDM Architecture with Frequency Time De-Interleaver (FTDI).

FSM Combinational logic units are a type of logic circuit whose output is a pure function of the present input only. Finite State Machines, used in sequential logic, have outputs that depend on both the present input as well as the history of the input. A sequential logic unit which 1, Takes an input and a current state 2, Produces an output and a new state. It is called a Finite State Machine because it can have, at most, a finite number of states.

It is composed of a combinational logic units are a type of logic circuit whose output is a pure function of the present input only.

The acquisition operation is realized by means of a synchronization block, which should be able to perform reliable frame detection (FD), estimations for the carrier frequency offset (CFO) and symbol timing offset (STO). The channel correction operation is needed to estimate and compensate the channel transfer function (CTF), provided that orthogonally has been restored to a great extent by the synchronizer. The final goal is to supply the decoding and demodulator block with In-phase and quadrature-phase components of the signal that are as similar as possible to the originals**.**

Finite state machine are used to model complex logic in dynamic systems. Examples of this complex logic include, In a digital circuit, an FSM may be built using a programmable logic device, a programmable logic controller, logic gates and flip flops or relays. More specifically, a hardware implementation requires a register to store state variables, a block of combinational logic which determines the state transition, and a second block of combinational logic that determines the output of an FSM.

A state is a description of the status of a system that is waiting to execute a transition. A transition is a set of actions to be executed when a condition is fulfilled or when an event is received. For example, when using an audio system to listen to the radio (the system is in the "radio" state), receiving a "next" stimulus results in moving to the next station. .

A low-density parity-check (LDPC) code is a linear error correcting code, a method of transmitting a message over a noisy transmission channel.

LDPC codes are finding increasing use in applications requiring reliable and highly efficient information transfer over bandwidth or return channel-constrained links in the presence of corrupting noise. Although implementation of LDPC codes has lagged behind that of other codes, notably turbo codes, the absence of encumbering software patents has made LDPC attractive to some.

VI. SIMULATION RESULTS

The BER plot of the OFDM receiver for an additive white Gaussian noise (AWGN) channel with soft-output LDPC FEC, when the de-interleaver memory is fault free. The quasi-error-free (QEF) point is defined as the maximum acceptable BER for which the application or the user does not perceive any degradation in performance.

The proposed strategy introduces a single multiplexer latency overhead on read and write operations and a configurable area overhead dominated by external-to-memory fault registers of size M/i bits, where M is the number of memory rows and i is an integer between 1 and M, inclusive.

Repair technique is different in the sense that it seeks to minimize the impact of embedded memory faults through permutation of high-sensitivity regions in addition to employing downstream soft-output LDPC decoders for correcting memory faults rather than using costly redundancy in the form of spare rows and columns or local ECC for memory repair..

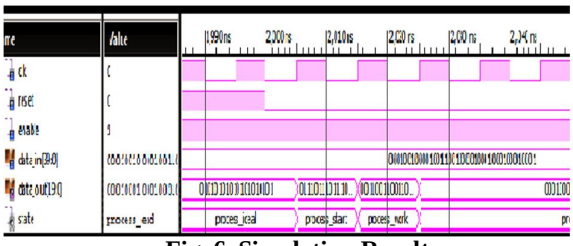

Fig. 6 .Simulation Result.

Memory repair SAFs were considered, the repair technique is not limited to hard memory faults and can also be applied to soft faults induced by reducing memory supply voltage in order to lower the power consumption in addition to an RF tuner card used to interface to the channel emulator and an external-to-FPGA SRAM memory chip used to store the de-interleaver data because of its large memory requirements.

A finite state machine is a model of a reactive system. The model defines a finite set of states and behaviors and how the System transitions from one state to another when certain conditions are true. Here attached the simulation results and plot the graph of a bit error rate and also packet error rate with respect to signal-to-noise ratio.

A fault mask is used to introduce bursts of alternating s-a-0 and s-a-1 faults of length, distributed throughout every group of 190 OFDM symbols, before the data are written into the functional SRAM chip, acting as a faulty de-interleaver memory of the architecture.

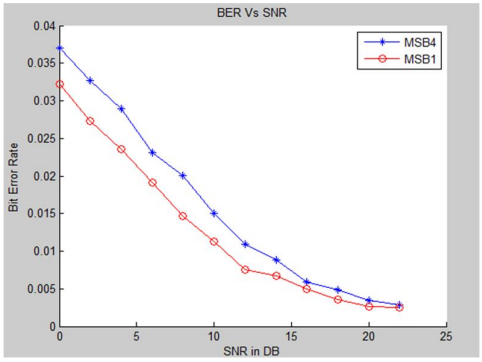

Fig. 7. BER vs SNR.

The advantages of the proposed method are memory area savings achieved by eliminating redundant rows and columns, a single multiplexer delay overhead, configurable area overhead, a simple interface with an existing MBIST infrastructure, and programmable sensitivity regions to minimize the impact of embedded memory faults through permutation of high- sensitivity regions.

A finite state machine is a model of a reactive system. The model defines a finite set of states and behaviors and how the system transitions from one state to another when certain conditions are true.

The FSM based address generator operates at higher frequency and can provide better FPGA resource utilization [9]. Use of internal memory always provides better results in terms of memory access time, power consumption and real estate occupancy of circuit board [13] compared to external memory.

This shuffled decoder can achieve comparable hardware efficiency compared to the proposed layered decoder. The decoder [20] is required to achieve a similar FER performance compared to using layered decoding. Reduce the memory fault by reducing the occupation of memory. Twice to increase the speed compared to existing soft memory techniques compared to the FSM soft memory techniques. Gain was also increased upon the references.

VII. REPORT ANALYSIS

Distinguish between previous techniques and proposed techniques. As compared to the parameters are techniques, Techniques, architecture, area, speed, power and gain.

In previous, we observe only on the Memory architecture of the OFDM system, and also predict the value of area, speed, power and gain, utilizing soft memory repair strategy. This strategy was used to avoid the delay, and also reduce the memory fault of the system. A soft memory repair strategy for baseband signal processing systems without redundant spare rows and columns.

Proposed techniques implement memory architecture on the OFDM system, and also observe the overall performance of the system.

Table. II. Comparison with existing Methods.

PARAMETER	EXISTING	PROPOSED
Technique	Soft Memory Repair Strategy	FSM based Memory Repair Strategy
Area	238416 KB	227520KB
Speed	1.872ns	2.067 ns
Power	0.754	0.4072
Gain	0.15 db	0.52db
Architecture	Implement on Memory Architecture	Memory architecture implement on OFDM System.

In Tab 2.measure the value of area, speed, power and gain, utilizing FSM based soft memory repair strategy. Here tabulate the values corresponding to the previous and proposed methods.

VIII. CONCLUSION

A FSM soft memory repair strategy for baseband signal processing systems without redundant spare rows and columns has been proposed. The proposed repair strategy saves implementation costs by eliminating redundancy and local error correction at the system level and improves decoding performance in the presence of memory faults by permuting the data so as to minimize the impact of memory faults on the BER. The effectiveness of the proposed repair technique is demonstrated on a multi- megabit de-interleaver also implemented on OFDM .The proposed technique introduces a single multiplexer delay overhead and a configurable area overhead of M/ i bits, where M is the number of memory rows and *i* is an integer from 1 to *M* , inclusive errors for an AWGN channel. In Future enhancement to reconfigure the entire OFDM system Architecture with Frequency Time De-Interleaver (FTDI) to achieve high gain, speed and reduction of memory fault and area.

REFERENCES

[1] S.-K. Lu, C.-L. Yang, Y.-C. Hsiao, and C.-W. Wu, "Efficient BISR techniques for embedded memories considering cluster faults," *IEEE Trans. conf, Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 2, pp. 184*–193, Feb. 2010.

[2] Jayarani, M.A., Jagadeeswari, M." *A novel fault detection and correction technique for memory applications*" Computer Communication and Informatics (ICCCI), 2013 International Conference on 4-6 Jan. 2013

[3] A. van de Goor, C. Jung, S. Hamdioui, and G. Gaydadjiev, "Low-cost, customized and flexible SRAM MBIST engine," in *Proc. Int. Symp. Des. Diag. Electron. Circuits Syst., 2010.*.

[4] F. J. Kurdahi, A. M. Eltawil, P. Young-Hwan, R. N. Kanj, and S. R. Nassif, "System-level SRAM yield enhancement," in *Proc. Int. Symp. Qual. Conf, Electron. Des., Mar. 2011.*

[5] S. K. Thakur, R. A. Parekhji, and A. N. Chandorkar, "On-chip test and repair of memories for static and dynamic faults," in *Proc. Int. Test Conf., 2012, pp. 1–10.*

[6] M. Ottavi, L. Schiano, X. Wang, Y.-B. Kim, F. J. Meyer, and F. Lombardi,"Evaluating the yield of repairable SRAMs for ATE," *IEEE Trans.conf, Instrum. Meas., vol. 55, no. 5, pp. 1704–1712, Oct. 2011*.

[7] R. Dekker, F. Beenker, "Fault modeling and test algorithm development for static random access memories," in *Proc. IEEE Int. Test Conf., Sep 2012*.

[8] S.-K. Lu and C.-H. Hsu, "Fault tolerance techniques for high capacity RAM," *IEEE Trans.conf, Rel.*, vol. 55, no. 2, pp. 293–306, Jun. 2011.

[9] S. K. Thakur, R. A. Parekhji, and A. N. Chandorkar, "On-chip test and repair of memories for static and dynamic faults," in *Proc. Int. Test Conf.*, 2012, pp. 1–10.

[10] F. J. Kurdahi, A. M. Eltawil, P. Young-Hwan, R. N. Kanj, and S. R.Nassif, "System-level SRAM yield enhancement," in Proc. Int. Symp. Qual. Conf,Electron. Des., Mar. 2012, pp. 178–184.

[11] Transmission System for Digital Terrestrial Television Broadcasting, Standard STD-B31, Nov. 2011.

[12] J. L. Ramsey, "Realization of optimum interleavers," *IEEE Trans.conf, Inf. Theory*, vol. 16, no. 3, pp. 338–345, May 2012.

[13] D. Forney, "Burst-correcting codes for the classic bursty channel," *IEEE Trans.conf, Commun. Technol.*, vol. 19, no. 5, pp. 772–781, Oct. 2009.

[14] J. G. Proakis and M. Salehi, *Digital Communications*, 5th ed. New York: McGraw-Hill, 2010.

[15] E. R. Berlekamp and P. Tong, "Interleavers for digital communications," U.S. Patent 4 559 625, conf, Dec. 17, 2009.

[16] C. Stapper, F. Armstrong, and K. Saji, "Integrated circuit yield statistics,"*Proc. IEEE*, conf, vol. 71, no. 4, pp. 453–470, Apr. 2010.

[17] A. van de Goor, C. Jung, S. Hamdioui, and G. Gaydadjiev, "Low-cost customized and flexible SRAM MBIST engine," in *Proc. Int. Symp.conf, Des. Diag. Electron. Circuits Syst.*, 2010, pp. 382–387.

[18] S.M.Al-Harbi and S. K. Gupta, "An efficient methodology for generat- ing optimal and uniform march tests," in *Proc. VLSI Test Symp.*, 2012.

[19] OFDM for Optical Communications Jean Armstrong, Senior Member, IEEE 2011.

[20] Optimal Training Signals for MIMO OFDM Channel Estimation Hlaing Minn, *Member, IEEE conf* and Naofal Al-Dhahir

[21] Y.-L. Ueng, Y.-L. Wang, L.-S. Kan, C.-J. Yang, and C.-J. Chen "Jointly designed architecture-aware LDPC convolutional codes and memory-based shuffled decoder architecture," *IEEE Trans conf. Signal Process.*, vol. 60, no. 8, pp. 4387–4402, Aug. 2012.